

**WHAT IS CLAIMED IS:**

1. A parallel processing system comprising:
  - N task orientated processing devices, wherein N is greater than 1 and each of the task-oriented devices providing a particular function;
  - M buffers, M greater than 1, each one adaptable to operate in a plurality of different phases operatively coupled to the N task orientated processing devices; and
  - Time Division Multiplex Control mechanism operatively connected to the M buffers and imposing respective ones of the different phases on said M buffers.
2. The parallel processing system of Claim 1 wherein M = N.
3. The parallel processing system of Claims 1 or 2 wherein the particular function includes cryptography.
4. The parallel processing system of Claims 1 or 2 further including an input bus operatively coupled to the M buffers;  
an output multiplexer operatively coupled to outputs of the M buffers; and  
an output bus coupled to the output multiplexer.

1       5. The parallel processing system of Claim 1 wherein the plurality of different phases  
2            include a Fast Write Phase, a Slow Read Phase, a Slow Write Phase and a Fast Read  
3            Phase.

1       6. The parallel processing system of Claim 5 wherein said each one of the M buffers further  
2            includes a slow write port receiving data if said each one of the M buffers is in the Slow  
3            Write Phase, a slow read port providing data if said each one of the M buffers is in the  
4            Slow Read Phase, a fast write port receiving data if said each one of the M buffers is in a  
5            Fast Write Phase and a Fast Read Phase providing data if said each one of the M buffers  
6            is in a Fast Read Phase.

1       7. The parallel processing system of Claim 4 wherein the Time Division Multiplex  
2            mechanism includes one TDM slow read address generator operatively coupled to at least  
3            one of the M buffers, one TDM Slow Write address generator operatively coupled to the  
4            at least one of the M buffers, one TDM Fast Read address generator operatively coupled  
5            to the at least one of the M buffers, and at least one TDM fast write address generator  
6            operatively coupled to said at least one of the M buffers; and  
7            a TDM Control circuit arrangement generating an output MUX control signal that  
8            drives said output multiplexor, a TDM Read Reset signal that drives the TDM slow read  
9            address generator and the at least one TDM Fast read address generator and a TDM write  
10          reset signal that drives the TDM fast write address generator and the TDM slow write

11 address generator.

1 8. The parallel processing system of Claim 7 wherein the TDM address generator includes a

2 binary counter;

3 an address bus operatively coupled to the binary counter;

4 a decoder operatively coupled to the address bus;

5 an inverter operatively coupled to the decoder;

6 an OR gate having a first input coupled to the inverter and a second input coupled  
7 to a Reset signal; and

8 an AND gate having a first input coupled to the OR gate, a second input coupled  
9 to a clock line and an output coupled to the binary counter.

1 9. The parallel processing system of Claim 7 wherein the TDM control circuit arrangement  
2 includes

3 a time base free running counter;

4 a TDM Reset Decoder operatively coupled to the output of the time base, free

5 running counter;

6 a circuit arrangement that monitors space available in each of the M buffers and  
7 outputs a control pulse if the available space is less than the space required to store a  
8 predetermined size data block;

9 a delay line; and

10 a buffer counter operatively coupled to the delay line and the circuit arrangement.

1 10. A parallel processing method including the acts of:

2 providing at least one process engine that provides a predetermined task;

3 providing at least one buffer operatively coupled to the process engine;

4 putting the at least one buffer in a fast write mode wherein data is received and

5 written into said buffer at a first speed;

6 putting the buffer in a slow read mode wherein data is read from the buffer into  
the at least one process engine at a second speed;

7 activating the at least one process engine to process data read out of the buffer;

8 putting the at least one buffer in slow write mode wherein processed data is  
written into the buffer from the at least one process engine at a third speed; and

9 putting the at least one buffer in a fast write mode wherein processed data is read  
out of the buffer at the same speed and sequence as the speed and sequence at which the  
10 data was received.

11. The method of Claim 10 wherein the at least one process engine includes a cryptographic  
12 unit.

1       12. A system comprising:

2                  at least one buffer having a first connection that ports to a network, a second

3                  connection that ports to a network, a third connection that ports to a process and a fourth

4                  connection that ports to the process; and

5                  a control circuit that generates a Fast Write Phase in which data is received at the

6                  first connection at a first speed, a Slow Read Phase at which data is transferred from the

7                  buffer through the third connection at a second speed, a Slow Write Phase in which data

8                  is written from the fourth connection into the buffer at the second speed and a Fast Read

9                  Phase in which data is transferred from the buffer to the second connection at the first

10                 speed.

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12       13. The system of Claim 12 further including a process engine operatively coupled to the

13                  third connection and the fourth connection.

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15       14. The system of Claim 12 wherein the process engine includes a cryptographic unit.

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17       15. The parallel processing system of Claim 9 wherein the predetermined size data block

18                  includes a data frame or data packet.

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20       16. The parallel processing system of Claim 15 wherein the space monitoring circuit

21                  arrangement includes a boundary MUX having an input from the buffer counter and a

3           plurality of inputs of boundary signals one from each buffer indicating address reached in  
4           each buffer at end of fast write phase;  
5           a subtractor responsive to output signal from the boundary MUX and output  
6           signal from the time base counter; and  
7           a comparator responsive to an output signal from said subtractor and a signal  
8           indicating length of the data frame.

17. The parallel processing system of claims 1 or 2 wherein the particular function includes  
any data processing system.

18. The parallel processing system of claims 1 or 2 wherein the particular function includes  
any data processing function whose processing time is proportional to frame length.